

CLAIMS:

What is claimed is:

1. A level shifter comprising:
a first inverter having a first threshold voltage; and
a second inverter having a second threshold voltage, the second threshold voltage
5 being greater than the first threshold voltage by at least a predetermined amount,
wherein the first inverter and the second inverter are cross-coupled.
2. The level shifter of claim 1 wherein:
the first inverter has a first configuration of transistors and the second inverter has a
second configuration of transistors;
10 the second configuration includes an additional transistor not found in the first
configuration.
3. The level shifter of claim 2 wherein the additional transistor is an N-channel
transistor.
4. The level shifter of claim 2 wherein the predetermined amount is at least one fourth or
15 greater of a gate-to-source voltage of the additional transistor.
5. The level shifter of claim 2 wherein the additional transistor is an N-channel
transistor, the N-channel transistor including a gate and a drain, wherein the gate is connected
to the drain.
6. The level shifter of claim 1 wherein:
20 the first inverter comprises a first P-channel transistor connected in series to a first N-
channel transistor;
the second inverter comprises a second P-channel transistor connected in series to a
second N-channel transistor, wherein a third N-channel transistor is connected in
series with the second N-channel transistor.

7. The level shifter of claim 1 wherein:
the first inverter consists essentially of two transistors connected in series;
the second inverter consists essentially of three transistors connected in series.

8. The level shifter of claim 1 further comprising:
a transistor have a gate coupled to an input of the level shifter and a current terminal,
a stress reduction transistor having a first current terminal coupled to the current
terminal of the transistor and a second current terminal coupled to an output of
the first inverter or an output of the second inverter.

9. The level shifter of claim 8 wherein:
the first inverter includes a transistor coupled to an output of a first voltage source and
the second inverter includes a transistor coupled to the first voltage source, the
first voltage source providing a first supply voltage;
the gate of the stress reduction transistor is coupled to the output of a second voltage
source to be biased at a voltage that is less than the first supply voltage.

10. The level shifter of claim 9 further comprising:
an input, a voltage of the input ranging between a low voltage and a high voltage,
wherein the gate of the stress reduction transistor is to be biased at a voltage that
is greater than the high voltage.

11. The level shifter of claim 1 wherein:
the first inverter includes a first transistor having a first current terminal coupled to an
output of a voltage source and a second current terminal coupled to an output of
the first inverter;
the second inverter includes a second transistor having a first current terminal coupled
to the output of the voltage source and a second current terminal coupled to an
output of the second inverter;
during power up of the voltage source, an output of the first inverter is pulled to a low
voltage state when a voltage of the output of the second inverter exceeds the
threshold voltage of the first inverter.

12. The level shifter of claim 11 wherein during power up of the voltage source, the output of the first inverter is pulled to ground when a voltage of the output of the second inverter exceeds the threshold voltage of the first inverter.

13. The level shifter of claim 1 comprising:

a non inverting output connected to an output of the second inverter.

14. The level shifter of claim 1 comprising:

a non inverting output connected to an output of the first inverter.

15. The level shifter of claim 1 comprising:

an inverting output connected to an output of the second inverter.

16. The level shifter of claim 1 comprising:

an inverting output connected to an output of the first inverter.

17. The level shifter of claim 1 further comprising:

a third transistor including a current terminal coupled to an output of the first inverter or an output of the second inverter, the third transistor including a gate coupled to an input of the level shifter;

a fourth transistor including a current terminal coupled to the output of the first inverter or an output of the second inverter, the fourth transistor including a gate; a third inverter having an input coupled to the input of the third transistor and an output coupled to the gate of the fourth transistor;

wherein the third inverter includes a transistor having a current terminal, wherein the current terminal is coupled to a first voltage source;

wherein the first inverter includes a first transistor having a current terminal coupled to a second voltage source;

wherein the second inverter includes a second transistor having a current terminal coupled to the second voltage source;

wherein the second voltage source powers up before the first voltage source.

18. The level shifter of claim 1 wherein:
the first inverter has a first configuration of transistors and the second inverter has a
second configuration of transistors;
the first configuration includes an additional transistor not found in the first
5 configuration.

19. The level shifter of claim 18 wherein the additional transistor is an P-channel
transistor.

20. The level shifter of claim 18 wherein the predetermined amount is at least one fourth
or greater of a gate-to-source voltage of the additional transistor.

10 21. The level shifter of claim 18 wherein the additional transistor is an P-channel
transistor, the P-channel transistor including a gate and a drain, wherein the gate is connected
to the drain.

22. The level shifter of claim 1 further comprising:
an output connected to one of an output of the first inverter and an output of the
15 second inverter;
drive circuitry connected to the output.

23. An integrated circuit including the level shifter of claim 1.

24. The integrated circuit of claim 23 further comprising:
a first circuit coupled to an input of the level shifter, the first circuit being powered
20 from a first voltage source;
a second circuit coupled to an output of the level shifter, the second circuit being
powered from a second voltage source;
wherein the second voltage source powers up before the first voltage source;
wherein an output of the level shifter is at a known voltage state prior to a powering
25 up of the first voltage source;
wherein the output of the level shifter is connected to one of an output of the first
inverter or an output of the second inverter.

25. The level shifter of claim 1 wherein:
the first inverter includes an input and an output;
the second inverter includes an input and an output;
the output of the first inverter is connected to the input of the second inverter and the
5 output of the second inverter is connected to the input of the first inverter.

26. The level shifter of claim 1 wherein:
the first inverter has a first transistor configuration with a first ratio of strength of a
first channel type transistor to strength of a second channel type transistor;
the second inverter has a second transistor configuration with a second ratio of
10 strength of a first channel type transistor to strength of a second channel type
transistor;
the first ratio is different than the second ratio by at least a predetermined amount.

27. The level shifter of claim 1 wherein:
the first inverter includes a first transistor of a first channel type;
15 the second inverter includes a second transistor of the first channel type;
wherein the first transistor has a gate dielectric of a different thickness than a gate
dielectric of the second transistor.

28. The level shifter of claim 1 wherein:
the first inverter has a first transistor configuration with a first transistor;
20 the second inverter has a second transistor configuration with a second transistor
corresponding to the first transistor of the first transistor configuration;
the first transistor has a strength different from a strength of the second transistor by at
least a predetermined amount.

29. A method of making a level shifter comprising:
25 providing a first inverter having a first threshold voltage; and
providing a second inverter having a second threshold voltage greater than the first
threshold voltage by at least a predetermined amount, wherein the first inverter
and the second inverter are cross-coupled.

30. The method of claim 29 wherein:
the first inverter has first configuration of transistors
the second inverter has a second configuration of transistors,
wherein the second configuration includes an additional transistor not found in the
5 first configuration.

31. The method of claim 30 wherein the predetermined amount is at least one-fourth or
greater of a gate-to-source voltage of the additional transistor.

32. The method of claim 30 wherein the additional transistor includes a drain and a gate,
the gate being connected to the drain.

10 33. The method of claim 29 wherein:
the first inverter has a first configuration of transistors;
the second inverter has a second configuration of transistors;
wherein the first configuration includes an additional transistor not found in the
second configuration.

15 34. A level shifter comprising:
a first inverter having a first configuration of transistors;
a second inverter having a second configuration of transistors;
wherein the first inverter and the second inverter are cross coupled;
wherein the second configuration includes an additional transistor not found in the
20 first configuration.

35. The level shifter of claim 34 wherein:
the first inverter has a threshold voltage and the second inverter has a threshold
voltage;
the threshold voltage of the first inverter is greater than the threshold voltage of the
25 second inverter by at least a predetermined amount.

36. The level shifter of claim 34 wherein:
the first inverter has a threshold voltage and the second inverter has a threshold
voltage;
the threshold voltage of the first inverter is less than the threshold voltage of the
5 second inverter by at least a predetermined amount.

37. The level shifter of claim 34 wherein the additional transistor is an N-channel
transistor.

38. The level shifter of claim 34 wherein the additional transistor is a P-channel transistor.

39. The level shifter of claim 34 wherein:
10 the first configuration includes a first transistor of a first channel type connected in
series with a second transistor of a second channel type;
the second configuration includes a third transistor of the first channel type connected
in series with a fourth transistor of the second channel type;
the additional transistor is a transistor of the second channel type and is connected in
15 series with the fourth transistor.

40. The level shifter of claim 34 wherein the additional transistor includes a drain and a
gate, wherein the gate is connected to the drain.

41. The level shifter of claim 34 further comprising:
an output, the output connected to an output of the first inverter.

20 42. The level shifter of claim 34 further comprising:
an output, the output connected to an output of the second inverter.

43. The level shifter of claim 34 further comprising:
an output, the output connected to an output of one of an output of the first inverter or
an output of the second inverter;
25 driver circuitry connected to the output.